Design and Performance Analysis of Soft Error Aware Random Access Memory

Synopsis Report of

Doctor of Philosophy

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This is to certify that the Thesis entitled **Design and Performance Analysis of Soft Error Aware Random Access Memory,** submitted by **Mr. Govind Prasad** to International Institute of Information Technology, Naya Raipur, is a record of bonafide research work under my supervision, and I consider it worthy of consideration for the Synopsis of the Thesis to be submitted in partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy of the Institute.

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Abstract

The radiation-hardened static random access memory (SRAM)-based memories are essential for space applications in near sub-threshold voltage, and it has challenges for the implementation of SRAMs for terrestrial applications at a higher frequency and low voltage region. The soft errors are the major problem of the SRAM-based memory used in high radiation environments (like satellite, aerospace) and terrestrial applications. Soft errors like single-node upset (SNU), single event double node upset (SEDNU), and multi-node upset (MNU) are severe issues with SRAM-based memory used in high radiation conditions. Modern SRAM-based memory becomes increasingly vulnerable to radiation-induced errors, often termed soft errors, as process technology continues to downscale. As technology scaling, the decreasing supply voltage and internal node capacitance of the circuit make the critical charge needed to upset the logic state of a circuit node much smaller, increasing the vulnerability of soft error. A soft error has become a significant concern not only for integrated circuits in aerospace but also for terrestrial applications. Hence, there is a need to develop radiation-hardened-based (RHBD) SRAMs to build highly dependable processors. In this work, soft error-aware RAMs have been proposed to address the challenges associated with RAMs at advanced technology nodes. The proposed SRAM can be resilient to any single node upset, single event double node upset, and multi-node upset at its storage nodes. The proposed RHBD SRAMs are checked and compared at a low voltage region under process variations. The simulation result shows that the proposed SRAMs have the better power cost, latency, write failure probability, and area among many considered SRAMs. The obtained observations demonstrate that one of the proposed SRAM can recover not only from SNUs but also from MNUs irrespective of the upset polarity. Also, the proposed SRAM has the highest soft error immunity and better hold, write and read stability among many considered SRAMs. Also, the figure of merit, probability of particle strike, sensitive area, probability of failure comparison, and Monte Carlo analysis of SRAMs validate that the proposed SRAMs are the better choice for sub-nanometer aerospace and terrestrial applications. Further, soft error-aware radiation-hardened RAM has been proposed using magnetic RAM (MRAM). The CMOS scaling makes it more challenging to handle soft errors caused by radiation. Along with MRAM give significantly less leakage current, non-volatility, and radiation-resilient. The proposed MRAM soft error-tolerant, low-power, non-volatile, and high-performance MRAM incurs a slight overhead in design while offering complete robustness against SNUs.

Keywords

Circuit reliability, critical charge, multiple-node upset, radiation hardened based design, single-node upset, soft-error-aware, static random access memory (SRAM).

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1. Introduction

Modern random access memory becomes increasingly vulnerable to radiation-induced errors, often termed soft errors, as process technology continues to downscale [1]. Radioactive particles like neutrons or alpha particles in terrestrial contexts can produce soft errors [2]. As technology scaling, the decreasing of supply voltage and internal node capacitance of the circuit make the critical charge needed to upset the logic state of a circuit node much smaller, increasing the vulnerability of single node upset (SNU) [3]–[5]. SEU has become a significant concern not only for integrated circuits in aerospace but also for highly terrestrial applications. Hence, there is an urgent need to develop radiation-hardened-based design (RHBD) RAMs to build highly dependable processors [6].

SRAM-based memories are extensively used to store the data in aerospace and terrestrial applications [7]. The soft errors like SNU and single event double node upset (SEDNU) as induced by high energy particles in the SRAMs are becoming one of the most severe issues [8]–[10]. The soft errors like single and double effect upset due to charge sharing are significant and detrimental for critical applications like satellite and medical equipment [11]. Also, the continuous scaling of technology reduces the space between transistors. As a result, multiple transistors can affect the charge deposited by a single-particle strike. The SEDNU becomes the main effect in emerging nano-meter technology due to energy particle strikes or charge sharing [12]. Hence, SEDNU, and multiple nodes upset may have a significant impact on the dependability of security applications, particularly in extreme radiation environments [13].

One of the best solutions to provide soft error tolerant SRAMs is to use radiation hardening techniques. The radiation hardening techniques do not require any modification in design rules and existing CMOS foundry processes [14]. These techniques or approaches are divided into the following three sub-approaches [7]. The first approach is based on the layout level. This approach is not convenient for sub-nanometer technologies because of its intricate design rules [7]. The second approach is based on the system level, as they apply error correction and detection codes (ECC) at the system level to protect from radiation effects [7]. This approach has the disadvantage of its high delay due to the more complex circuit of the decoder and encoder [15]. The third approach, circuit-level, is based on circuit changes. The circuit-level as referred RHBD can provide less delay with more resilience from soft errors [15]. The circuit-level approach is preferable over the layout and system-level because of its high resilience from radiation and high speed [15].

SRAM-based memory is frequently used because of its infinite reconfigurability, excellent performance, and CMOS compatible [16]. Moreover, SRAM-based memories are volatile and lose their configuration once the power is turned OFF [17]. In addition, SRAM memory is exceptionally susceptible to soft errors [18]. Consequently, the architecture of the circuits built on SRAM-based FPGAs is vulnerable to radiation [19]. Hence, whenever a charged particle hits an SRAM, it may change the logic level of the node. Leakage current and accompanying power usage rise when CMOS technology shrinks [20]. Currently, leakage current is a critical concern for designing large-scale CMOS circuits for sub-nanometer design [21]. Also, the CMOS scaling makes it more difficult to handle soft errors caused by radiation [22]. Along with its low leakage and CMOS compatibility, MRAM logic circuits might be an appealing alternative to SRAM-based logic. Additional benefits of MRAM-based logic compared to SRAM based are its non-volatility and radiation-resilient.

2. State of the Art: One of the best solutions to provide soft error tolerant SRAMs is to use radiation hardening techniques. The radiation hardening techniques do not require any modification in design rules and existing CMOS foundry processes [5]. These techniques or approaches are divided into the following three sub-approaches [5]. The circuit-level, referred radiation-hardened-based design (RHBD) can provide less delay with more resilience from soft errors [6]. The circuit-level approach is

preferable over the layout and system-level because of its high resilience from radiation and high speed [9]. The triple modular redundancy (TMR) is a commonly used circuit-level approach to protect the memory from radiation effects like a soft error. The main drawbacks of TMR are high power dissipation and large area [1]. The most popular circuit-level hardening techniques are proposing new hardened SRAM cells [3]. In recent years, researchers have reported many RHBD cells like DICE-12T [1], QUATRO-10T [2], QUATRO-12T [3], RHBD10T [4], QUC.-12T [5], and RHBD-12T [6] to provide soft errors resilience, especially for SEU. Significantly, few researchers have reported the RHBD SRAM cells for SEDNU/MNU tolerance like RHBD-14T [7], SEA-14T [13], RHBD-15T [14], and DNUSRM [15] with compromising the power, stability, and speed. Overall, while designing a radiation-hardened circuit, there is a trade-off between soft error tolerance, power, and speed [1]-[5].

Magnetic tunnel junctions (MTJs) are immune against radiation-induced soft errors [16]-[19]. However, as the mentioned magnetic circuits need a CMOS component for read and write operations, the issue of soft error still exists for magnetic-based devices [20]-[22]. In [18]-[20], it has been shown that magnetic-based latches suffer from soft error in read operation and a wrong logic value would be resulted by the read circuit. Therefore, the previously proposed MRAMs [16]-[20] can resolve the issue of high standby power consumption and also the volatility of the conventional SRAMs. However, the subject of radiation hardening is not considered and RAMs are still vulnerable to radiation effects. The MRAMs presented in [21], and [22] give SNU upset resilience but it consumes more area and power cost. A brief overview of soft-aware random access memories is reported in Table I.

Table I: Brief overview of the soft error-aware RAMs

Soft errors	RAMs	Methodologies/Remarks
SNU Aware	DICE12T [1]	Large area overhead, more power cost, and more read/write.
	QUAT.10T[2]	Write failure at a higher frequency due to process variation.
	QUAT.12T[3]	Reliable write operation and same area compared to QUAT.
	RHBD10T [4]	Area-efficient, and write failure at a higher frequency
	QUC.10T [5]	Soft error resilience, write failure at a higher frequency
	QUC.12T [5]	Soft error resilience, more power cost and read/write delay
	RHBD12T [6]	Its substantial delay and leakage current restrict its use.
SEDNU Aware	RHBD13T [8]	High read/write delay and leakage current restrict the use.
	RSP14T [9]	Layout optimization techniques and less stability.
	SRRD12T [10]	Highest read stability due to read decoupled technique.
	EPD12T [11]	Recovers from SEDNUs at its internal node-pair.
	RHD14T [12]	High SEDNU critical charge, more static power, and delay.
MNU Aware	SEA14T [13]	Fully recovery from MNUs induced at the internal node-pair.
	RHBD15T [14]	Layout optimization techniques and more area overhead.
	DNUSRM [15]	It completely self-recovers from any possible DNU/MNU.
MRAMs	17T MRAM[16]	Not soft error-tolerant, data are recalled with no error even in the presence of a mismatch.
	7T MRAM [17]	
	13T MRAM [18]	Zero leakage power, low-power, and better performance computing. Magnetic-based RAMs suffer from soft errors in read operation and a wrong logic value would have resulted.
	13T MRAM [19]	
	21T MRAM [20]	
	26T MRAM [21]	Low-power, non-volatile, and high-performance M-latch incurs a little overhead and full robustness against SEUs.
	27T MRAM [22]	

3. Motivation and Objectives: Soft errors induced by particle radiation are becoming an increasingly critical threat to the reliability of memories fabricated in nano-scale CMOS technologies [5]. Soft errors are caused by a particle-induced charge which is derived from direct ionization from heavy ions and indirect ionization from protons and neutrons [3]–[6]. An energetic particle passes through the sensitive node of a semiconductor device. It frees electron-hole pairs along its path as it loses energy. The electric field present in a reverse-biased junction depletion region can separate electron-hole pairs. The particle-induced charge is very efficiently collected through drift processes leading to an accumulation of extra charge at the sensitive node [7]–[11]. When the amplitude of the accumulated charge is enough and the time is long enough, it can generate a large voltage transient pulse which temporarily changes the value of the sensitive node (Fig. 1(a)). In addition, the sensitive areas of the semiconductor devices are the strongly reverse-biased diffusion areas where the induced transient current flows from the N-type diffusion to the P-type diffusion [7]. As a result, when a radiation particle strikes PMOS, a positive transient pulse is generated, as shown in Fig. 1(b); on the contrary, when a radiation particle strikes NMOS, a negative transient pulse is induced, as shown in Fig. 1(c).

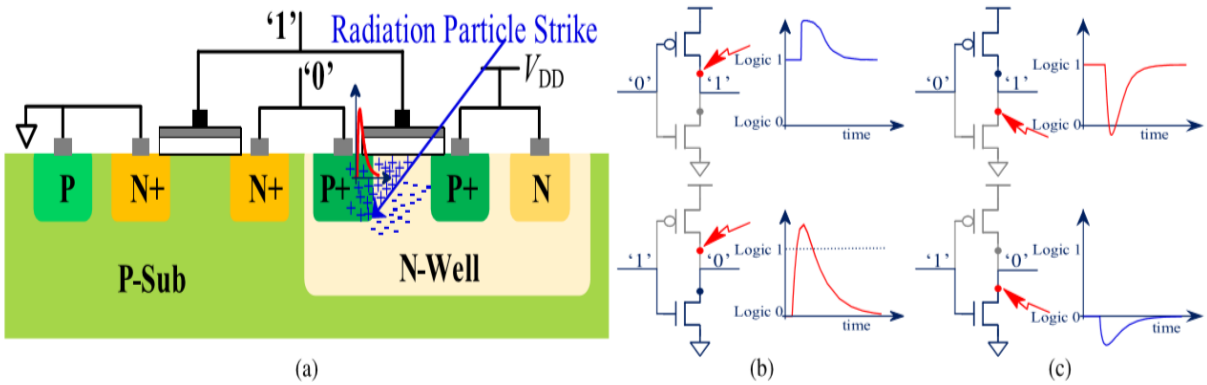

Fig. 1: (a) Device physics for the generation of a transient voltage pulse when a radiation particle strikes the PMOS of an inverter, (b) Positive transient pulse generation when a radiation particle strikes the PMOS, and (c) Negative transient pulse when a radiation particle strikes the NMOS [7].

The objective of the report is motivated by the points mentioned above are listed below:

1. To design, a single node upset resilience radiation-hardened based SRAMs with optimized parameters, better writability, and readability.
2. To investigate the charge sharing effect among nodes and design a single event double node upset resilience SRAM-based memory.
3. To design, a low-cost, highly reliable, multi-node upset-aware SRAM memory.
4. To study the compatibility of emerging devices like STT-MRAM with CMOS.
5. To design, a new radiation-hardened random access memory for single node upset awareness using a hybrid of STT-MRAM and CMOS technology.

4. Details of Research works:

4.1 Proposed Work Chapter 2:
SNU Resilience RHBD SRAM Cell

4.1.1 Design and Analysis of 10T-Boosted Radiation Hardened SRAM Cell

The significant disadvantages of the DICE-12T [1] and QUAT. 12T [3] is its large area and high power consumption. J. Guo et al. proposed and designed a 10T SRAM cell as delineated in Fig. 2(a), to address high power consumption and area problems [4]. To check the working operation of the 10T SRAM cell in the worst scenario (SS process and 85◦C temperature), the statistical analysis (Monte Carlo (MC)) has been performed during the read and write mode of the SRAM cell. The 10T SRAM cell shows

perfect read operation even in the worst scenario, and it is not able to get any read failure. During the write mode, when a large number of MC simulations are performed, the 10T cell shows a large number of write failures due to process variation at different process corners and 85◦C temperature. The transient response of 10T SRAM cell at a higher frequency depicts in Fig. 2(b) at 45 nm CMOS technology. Fig. 2(b) clearly shows that the 10T cell is not able to perform write operation at a higher frequency due to the process variation.

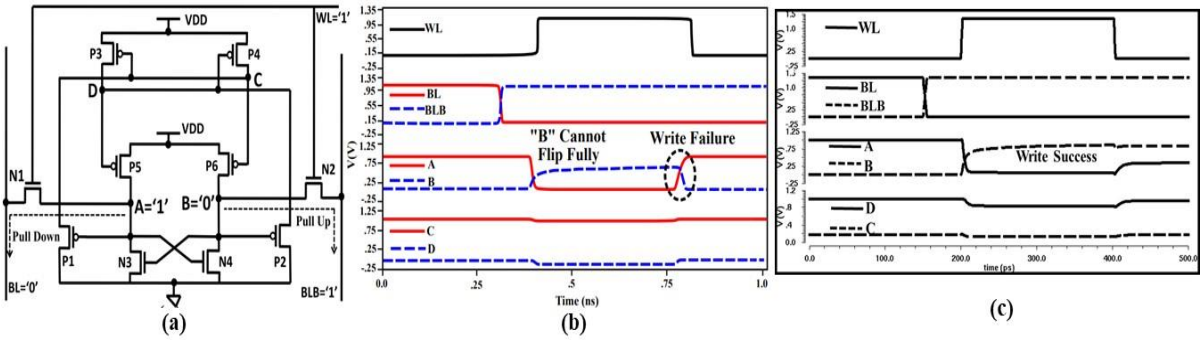

Fig. 2. (a) Schematic diagram of the 10T-SRAM cell, (b) Transient responses of the 10T-SRAM cell, which depict the write failure, and (c) Transient response of the 10T-boosted cell, which shows successfully write operation.

In the 6T SRAM cell, the output node "A" pulls down through access transistor N1, which turns "ON" pull-up transistor P2 of the 6T cell. This directly pulls up the output node "B" to supply voltage through transistor P2. Also, the access transistor N2 helps to pull up the output node "B," but due to the weak strength of NMOS (N2), this effect is small. So node "B" is completely pulled up by transistor P2. Fig. 2(a) shows the reason behind the write failure of the 10T SRAM cell. In the 10T SRAM cell also, the output node "A" pulls down through access transistor N1. As the output "A" pulls down, the gate voltage of N4 also gets reduced, which makes the transistor N4 weaker. And node "B" pulls up through transistor N2 as NMOS gives weak '1', so the flipping occurs at the output nodes. However, in 6T SRAM output nodes pulls-up through PMOS transistor P2. Hence weak NMOS (N2) and high delay are the reason behind the write failure of the 10T SRAM cell at high frequency under process variation.

The 10T-SRAM cell [4] is facing a poor writability problem. And it is not suitable for cache memory due to the poor writability of the 10T SRAM cell. Negative biasing bit-line (BL) [17] and boosting word-line (WL) [18] are the popular approaches to increase the writability of the SRAM. However, the access transistors (N1, N2) of the 10T SRAM-cell, as indicated in Fig. 2(a), have weak pull-up strength, which more affects the writability under process variation of 45 nm CMOS technology. Therefore, the boosted bit-line and the word line are a better way to enhance the strength of access transistors N1 and N2 for better writability under process variation. In this work, the first time combination of both boosted WL and BL of 10T SRAM cell is designed and verified by MC Simulation. When the 10T boosted SRAM cell is checked by MC Simulation during read and write mode, it shows no write and read failure up to 0.5 GHz. So boosted 10T SRAM is the better choice for cache memory for sub-nanometer technology under high radiation environments like aerospace and satellite. The limited boosted and biasing voltage is applied as more boosted, and biasing affects oxide reliability. The transient responses of the 10T boosted cell, which show the successfully written operation of the cell shown in Fig. 2(c).

4.1.2 Low Power and Write-Enhancement RHBD 12T SRAM Cell

In this work, the novel 12T RHBD SARM cell has been proposed to overcome the soft errors (single event upset) and writability failure issue at a higher frequency. The proposed cell, as shown in Fig. 3(a), consists of twelve transistors. The 10T SRAM cell [4] is facing write failure at a higher frequency. So two extra transistors N3 and N4 have been added to the 10T cell in the proposed cell to avoid the write failure. The We-Quatro and DICE cell consists of twelve transistors, where four (P1-P4) PMOSs, and eight (N1-N8) NMOSs, respectively. As it has, more NMOSs and due to the structure of design during reading and write mode, the maximum number of transistors is in active mode, and hence, it consumes more power. Therefore, to achieve high soft error and less power consumption, the proposed cell has

been designed using more PMOSs with a different configuration of transistors. The power and area cost has been reduced. The critical charge has been improved respectively due to the small size of transistors (all transistors are the same size except P3 and P4 (2.1×)) and more number of PMOSs. The write speed and write SNM have been improved due to added extra N3 and N4 access transistors. The larger P3, P4, and connection of the transistors are responsible for higher hold stability.

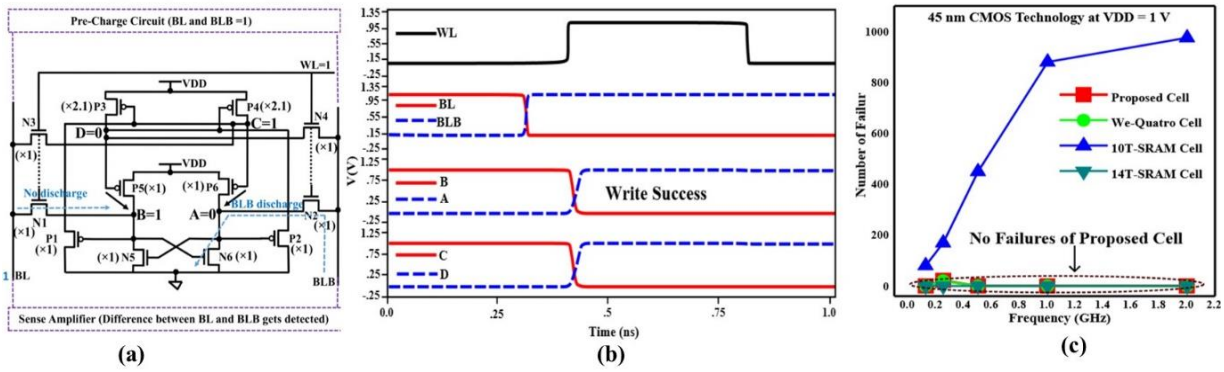

Fig. 3. (a) Schematic diagram of the proposed SRAM cell, (b) Transient responses of the proposed cell, which shows successfully write operation of the cell at a high frequency (1 GHz), and (c) 1000 MC Simulation of SRAM cells to compare writability at various frequencies and supply voltage equal to 1.0 V.

In retention mode, logic '0' is applied to WL. Under this condition, as WL = '0' all-access transistors N1-N4 will be "OFF". Hence the stored value at the output node in the latch will be disconnected from bit lines and there will be no changes in the output. Similarly, the circuit is connected from the bit lines and the logic signal of active high ('1') to WL is called active mode. During the read operation, the pre-charge circuit gives high voltage to both the BL = '1' and BLB ='1'. If the proposed cell holds a high value, then there is no discharge of BL voltage. But BLB voltage will be discharged, and the stored output is decreased as both the bit lines are connected to the differential sense amplifier, which gives the digital output. Now for a write operation, assume to write '1' on the proposed cell which is holding the value '0', then it needs to give BL = '1' and BLB = '0'. Under this condition, as WL = '1' transistors N1-N4 will be "ON", the transistors N6, P2, P4, and P5 will be "ON" so that the transistors P1, N5, P3, P6 will be "OFF" and the store output in the cell will change from value '0' to '1'. Hence, the write operation is performed successfully. Fig. 3 (b) shows the perfect operation of the proposed cell.

Suppose delicate node "B" of the proposed cell is affected by radiation (high energy particles touch the node "B") then the value stored in the output "B" ('1') flipped immediately to '0'. The transistors N6 and P1 will be switched "OFF" and "ON" respectively for a short period. In the proposed cell, as the size of P4 is larger than the P1 (2.1×), the maximum voltage from supply drops across transistor P4, and the value at node "C" is equal to '1'(previous). However, the gate of transistor P3 is connected to node "C". Hence P3 will always be "OFF". Due to "OFF" transistor P3, the voltage across node "D" is unchanged ('0'). The value ('0') at the node "D" makes the transistor P5 always "ON". Finally, the initial voltage is rolled over to node "B," which equals to '1'.

Initially, the output nodes "B" and "C" store the value '1' and the output node "A" and "D" store the value '0' by an assumption of the proposed cell. Now it has been written the opposite data during the write mode of the cell. The logic signal high ('1') has been applied to BLB and low ('0') to BL. Under this condition, the access transistors N1 and N3 are pulled down by the node voltages at "B" and "C," similarly the access transistor N2 and N4 have been pulled up by the output nodes "A" and "D". Fig. 10 shows successfully write operation of the proposed cell at 1 GHz. In Fig. 2(a), the 10T SRAM cell is not able to write at a higher frequency. The 10T SRAM cell is not able to provide full VDD potential to the output nodes "A" and "B" due to the weak pull-up of NMOS (N1 and N2). However, in the proposed cell, the extra added transistors N3 and N4 pull down the node "C" and "D" respectively. The potential at "C" and "D" turn "ON" the P6 and P5 respectively generate the nodes "A" and "B" to full VDD. This type of feedback boosts the writability of the proposed cell, as shown in Fig. 3(c). Hence, in this work, a 12T RHBD SRAM cell has been proposed for low voltage terrestrial applications. The proposed cell consumes less energy compared to all considered SRAMs.

4.2 Proposed Work Chapter 3:
SEDNU Resilience RHBD SRAM

4.2.1 Energy-Optimized and Soft-Error-Aware Read-Decoupled SRAM

In this work, a 14T energy-optimized soft error aware read decoupled (ESR-14T) SRAM cell has been proposed to overcome the single event upset (SEU) / single event double node upset (SEDNU). Soft errors like SEU and SEDNU are severe issues with SRAM-based memory used in high radiation conditions like aerospace applications. The SEU/SEDNU are caused by high-energy particles. The proposed ESR-14T gives better performance than other SRAM cells. The simulation results show that the ESR-14T cell can tolerate SEU/SEDNU. The ESR-14T cell has the highest read stability due to the read decoupling approach. Overall, the ESR-14T cell consumes less power, has less write delay, better stability, and has the highest critical charge than other cells. The area overhead and read delay are also better than many of the SRAM cells. Hence, with the improved balance of all parameters, the ESR-14T cell is more appropriate for crucial aerospace applications.

The circuit diagram and thin cell type layout of the ESR-14T cell are shown in Fig. 4 (a) and (b), respectively. In Fig. 4(a), the N3 and N4 (P9 and P10) are used as access transistors to connect storage nodes “A” and “B” (“C” and “D”) to the bit lines BL and BLB, respectively on activation of WWL (RWL). To explain the working principle of the ESR-14T, let us consider the logic ‘1’ is stored (“A”, “B”, “C”, “D” are ‘1’, ‘0’, ‘1’, ‘0’, respectively). The write word line (WWL), read word line (RWL), bit line (BL), and bit line bar (BLB) are fixed to ‘1’, ‘1’, ‘0’, and ‘1’, respectively, to write ‘0’ into the cell. The transistors P5, P6, P2, P7, N1, P9, and P10 are switched OFF, and P3, P4, P1, P8, N2, N3, and N4 are switched ON. As a result, node “B” (“A”) is charged (discharged) to ‘1’ (‘0’). To hold logic ‘0’ into the ESR-14T, the WWL/RWL is fixed to ‘0’/‘1’. The transistors P5, P6, P2, P7, N1, N3, N4, P9, and P10 are switched OFF, and P3, P4, P1, P8, and N2 are switched ON. As a result, the nodes “A” and “B” are not changed and hold the stored data. The read process begins with pre-charging bit lines to supply voltage and fixing RWL to ‘0’. To provide an uninterrupted read operation, WWL is set to logic ‘0’. The transistors P5, P6, P2, P7, N1, N3, and N4, are switched OFF while P3, P4, P1, P8, N2, P9, and P10 are switched ON. The bit lines are pre-charged to logic ‘1’ and P8, and P10 is switched ON. Hence BLB discharges. However, P7 is switched OFF, so there is no path to discharge BL and it is fixed to ‘1’. The sense amplifier detects the voltage difference among bit lines [5]. Notably, node pairs “A-B” are inaccessible throughout the reading process.

Single Event Double Node Upset (SEDNU) Tolerance Analysis: According to the upset physical mechanism [5], node “C” is robust against ‘1’ to ‘0’ upset (only ‘1’ to ‘1’ transient is possible). Hence, if the node pairs “A-C,” “BC,” and “C-D” are upset due to radiation strikes and charge sharing, then they will be recovered. As node “C” is insensitive to radiation effect. This case looks like SEU on nodes “A,” “B,” and “D” are recovered, as explained in subsection II-B (case-1, 2, and 3, respectively).

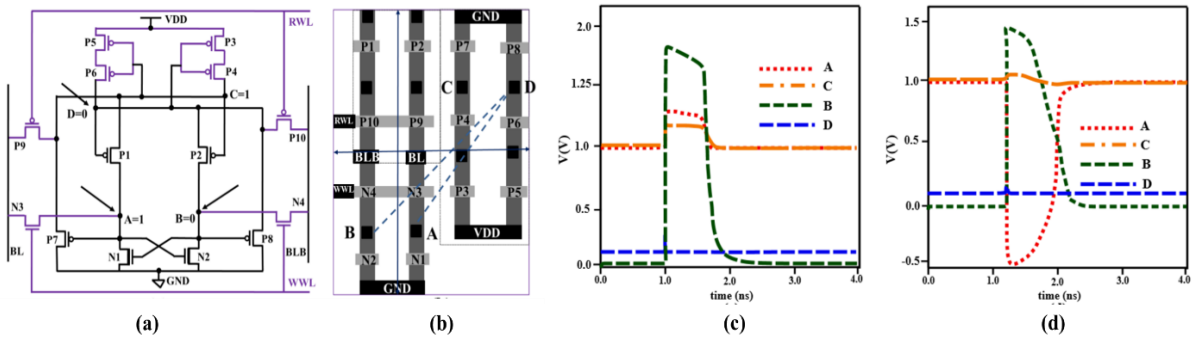

Fig. 4. (a) Circuit diagram (b) Thin cell type layout of the proposed ESR-14T SRAM cell, and (c) Soft error recovery when node “B,” and (d) “A-B” are affected simultaneously.

If the node pair “A-B” is upset due to radiation strikes and charge sharing, it will recover. Due to radiation hit on node pair “A-B” at the same time, the stored data at nodes “A” and “B” are temporarily

changed from ‘1’ to ‘0’ and ‘0’ to ‘1’, respectively. This is analogous to the scenario where node “B” is impacted by an SEU (subsection II-B, case-2). As a result, node pair “A-B” revert to their previous state. If node pairs “A-D” and “B-D” have enough charge deposited, the stored data at nodes “A” and “B” may be altered to ‘0’ and ‘1’ and “D” can be changed to ‘1’. As a result, the stored information in the cell might be flipped. Nevertheless, to shift the state of “B” and “D” nodes from ‘0’ to ‘1’ (i.e., ‘0’ to ‘1’ transient) at the drain of OFF PMOS, it is necessary to deposit a larger charge in comparison to ‘1’ to ‘0’ transient [6] and the possibility of occurring multi-node upset at node pairs “A-D” and “B-D” can be reduced by maintaining adequate distance between node pair “A-D” and “B-D” [7]. Furthermore, charge sharing can occur among NMOSs, PMOS-NMOS, and PMOSs unless they are close to 2 µm, 0.60 µm, and 1.62 µm, respectively [4], [6]. The proposed cell’s layout is designed with suitable separation to avoid charge sharing among nodes. The soft error recovery when node “B” and node pair “A-B” are affected is shown in Fig. 4 (c) and (d), respectively.

In this work, an ESR-14T SRAM cell has been proposed, which has the following advantages:

1) The ESR-14T cell can self-recover at all the sensitive nodes from all the possible SNUs/SEDNUs of both polarities. The splitting of PMOSs (P3, P4, and P5, P6) and more PMOSs in the ESR-14T are responsible for better critical charge (Q_c) than other cells.
2) The ESR-14T dissipates the lowest hold and total power due to the stacked structure. Also, in the ESR-14T, the P1 and P2 are connected to the gate of P6 and P4, respectively, instead of supply voltage being responsible for less power cost.
3) The ESR-14T has better stability than most cells due to the lower body effect and better size of transistors. Also, due to the read-decoupled of the ESR-14T, it is read upset-free.
4) The writability and write access time are also improved compared to other SRAMs due to the better pull-up ratio and poor driving ability of their internal nodes. The use of low threshold (Vth) MOSs (N1 and N2) in the ESR-14T is also responsible for better writability and write access time.

4.2.2 SRAM Cell with Enhanced Self-Recoverability from Soft Errors

The severe pain of technology reduction is its effect on neighboring nodes when high-energy particles strike at any device node. In this work, a 14T radiation-hardened-based SRAM cell has been proposed to overcome soft errors. The proposed cell gives better performance than other standard RHBD cells, even with the recently reported RHBD 14T cell. Simulation results show that the proposed cell can be resilience to any single event upset and single event double node upset at its storage nodes. This cell consumes less static and total power loss compared to all considered cells. The hold, read, and write stability increases compared to most of the considered cells. The higher critical charge of the proposed cell gives more robustness in the radiation environment. Hence, the better balance among the parameters makes the 14T proposed SRAM cell more suitable for critical terrestrial applications.

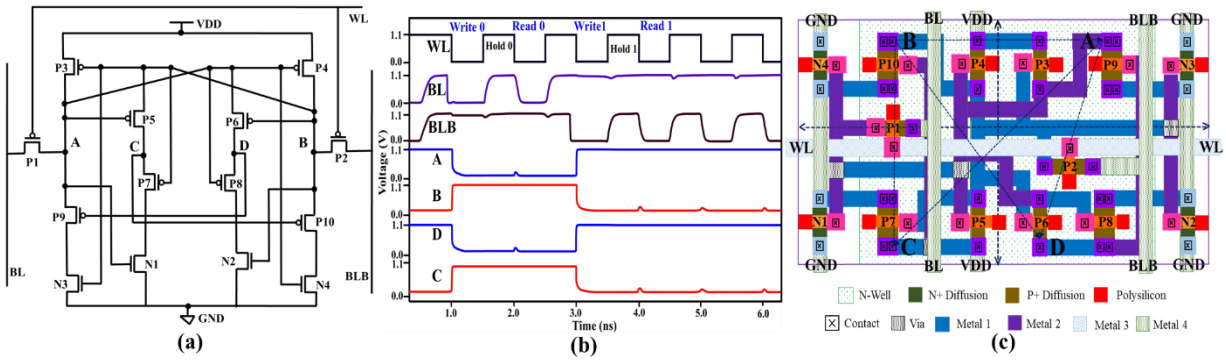

Fig. 5. (a) Circuit diagram, (b) Complete operational waveforms, and (c) Layout of the proposed SRAM cell.

In this work, a new RHBD-14T cell, as shown in Fig. 5(a), is designed. Based on physical phenomena and simulation results reported in [7], [12], the negative (‘1’ to ‘0’) and positive (‘0’ to ‘1’) transitory pulses can be generated whenever a radiation particle strikes the reverse-biased NMOS and PMOS transistors, respectively. Hence, the PMOSs P1 and P2 are used as access transistors to avoid negative

pulse changes from '1' to '0' at "A" and "B" due to a radiation particle. The proposed cell has four inverters. In all four inverters, the low threshold PMOS is added between NMOS and PMOS to minimize the charge sharing effect (to increase the robustness in terms of SEDNU) and to improve the voltage swing. The circuit diagram of the proposed 14T SRAM cell is shown in Fig. 5(a). In Fig. 5(a), the PMOSs P1 and P2 are used as access transistors to connect outputs "A" and "B" to the bit lines BL and BLB, respectively. The use of PMOSs as access transistors gives only positive transient ('1'→'1' or '0'→'1') at the output nodes "A" and "B" in the proposed cell. The novel 14T cell uses four inverters as follows Inverter 1 (P3, P9, N3), Inverter 2 (P5, P7, N1), Inverter 3 (P6, P8, N2), Inverter 4 (P4, P10, N4). A low threshold PMOS is added between a pull-down and pull-up MOS of a conventional inverter. In Fig. 5(a), the inputs of inverters are '1'→'0' flip immune due to output nodes being surrounded by PMOSs. As a result, the flipping of outputs gets reduced. The different parameters comparison of SRAMs are reported in Table II.

In the write operation, the PMOS access transistors P1 and P2 give strong high (VDD) and weak low (threshold-voltage) at the output nodes. Hence, the inverters or output of the cell provide a voltage swing between VDD and threshold voltage (V_{th}). Therefore, low threshold PMOSs (P7-P10) in the proposed cell improve the voltage swing. Also, the high threshold NMOSs (N1-N4) reduce the leakage current and enhance the stability. In the proposed cell, the source of PMOSs P5 and P6 are connected to the gate of PMOSs P3 and P4 instead of VDD, which decreases the current and thereby reduces the power cost. To explain the operations of the proposed SRAM cell in different modes, let us consider the logic '0' ("A", "B", "C", "D" are '0', '1', '1', '0', respectively) is stored. The operation of the proposed cell in different modes is listed as follows: To write logic '1' into the cell the word line (WL), bit line (BL), and bit line bar (BLB) are fixed to '0', '1', and '0', respectively. Transistors P3, P6, P7, P10, N1, and N4 are switched OFF and transistors P1, P2, P4, P5, P8, P9, N3, and N2 are switched ON. As a result, the nodes "A" and "B" are charged, discharged to logic '1' and weak '0', respectively.

Table II: Parameters comparison of SRAMs

SRAM Cells	Static Power (pW)	Dynamic Power (nW)	Total Power (μW)	Area (μm^2)	RAT (ps)	WAT (ps)	Sensitive Area (μm^2)	SEU Q_c (fC)	HSNM (mV)	RSNM (mV)	WSNM (mV)	No. of Failures	P_S
Proposed-14T	**28.23**	2359	**2.36**	**5.182**	**92.21**	**12.01**	**0.126**	**51.6**	**398**	**206**	**249**	**0**	**0.024**
RSP-14T [9]	33.02	2709	2.71	5.359	88.78	13.36	0.209	21.2	254	215	231	4861	0.039
RHBD-14T [7]	34.21	2659	2.66	5.293	97.51	11.59	0.191	34.1	381	147	203	1889	0.036
RHBD-13T [8]	39.82	2979	2.98	5.191	85.01	21.02	0.202	26.5	361	162	177	2456	0.038
QUC.-12T [5]	41.02	4509	4.51	5.059	81.52	11.31	0.213	12.3	304	186	193	4912	0.042
RHBD-12T [6]	32.82	2509	2.56	4.968	91.32	10.23	0.187	25.3	366	196	240	2689	0.037
QUAT.-12T [3]	38.23	3729	3.73	4.932	76.13	11.83	0.198	19.5	277	173	228	4683	0.040
DICE-12T [1]	36.52	2929	2.93	5.140	83.30	11.68	0.181	17.3	403	191	180	4793	0.035
SRRD-12T [10]	40.12	3849	3.85	4.982	94.63	18.53	0.165	33.8	372	217	186	1625	0.033
DNUSRM [15]	47.53	4779	4.78	6.691	91.53	14.63	0.315	63.8	421	153	236	0	0.047
SEA-14T [13]	32.52	2629	2.63	5.312	89.21	11.12	0.196	46.5	384	211	237	206	0.037
RHD-14T [12]	40.16	2849	2.85	5.268	93.02	13.21	0.136	31.6	340	169	229	2012	0.024
EPD-12T [11]	31.12	2539	2.54	5.021	89.23	12.32	0.192	41.2	283	201	239	521	0.037
Basic 6T	19.16	2009	2.01	0.396	69.23	13.03	-	-	301	166	198	-	-

Similarly, the write operation of logic '0' into the proposed cell is also performed. The simulated responses of the proposed cell for write '1' and '0' are delineated in Fig. 5(b). To hold logic '1' into the cell, as shown in Fig. 5(b), the WL is fixed to logic'1'.The transistors P3, P6, P10, P7, N4, and N1 are switched ON, and P1, P2, P4, P5, P8, P9, N3, and N2 are switched OFF. As a result, the nodes "A" and "B" are charged, and it holds the stored data. Similarly, to hold logic '0' into the cell is also performed. The simulated responses of the proposed cell for hold '1' and '0' are delineated in Fig. 5(c). To read logic '1' from the cell, the WL is fixed to '0', whereas BL and BLB are fixed to '1'. Transistors P1, P2, P3, P6, P7, P10, N1, and N4 are switched ON, and P4, P5, P8, P9, N3, and N2 are switched OFF. As the node "A" and BL has the same potential ('1'), no current flow through P1. However, the node "B" and BLB has different logic weak '0' and '1' respectively, so BLB will be discharged. The sense

amplifier will detect the difference voltage between BL and BLB and give the stored data. The simulated responses of the proposed cell for read '1' and '0' are shown in Fig. 5(c).

Single Event Double Node Upset (SEDNU) Tolerance Analysis: As the proposed cell's node "B" and "C" ('1') is surrounded by PMOSs, so only a positive transient is possible ('1' to '1'). Therefore, only "A" = '0', and "D" = '1' are the only sensitive nodes for the proposed cell. The proposed cell is SEU immune and SEDNU tolerant. It may be SEDNU immune if its layout maintains a minimum distance between sensitive node pairs, as reported in [5]. To evaluate the single event double node upset (SEDNU) tolerance capacity of the proposed cell, which has four nodes (A, B, C, D), six possible node pairs (A-B, A-C, A-D, B-C, B-D, C-D) are realized.

The SEDNU recovery of the proposed cell is illustrated in the following cases: Case 1 (SEDNU at node pair "A-B"): If the node pair "A-B" is upset due to radiation strikes and charge sharing, they will be recovered. However, node "B" is insensitive to the radiation effect. This case looks like SEU on node "A" is recovered, as explained in subsection II-B (case -1). Case 2 (SEDNU at node pair "A-C"): If the node pair "A-C" is upset due to radiation strikes and charge sharing, they will be recovered. However, node "C" is insensitive to the radiation effect. This case looks like SEU on node "A" is recovered, as explained in subsection II-B (case -1). Case 3 (SEDNU at node pair "B-C"): If the node pair "B-C" is upset due to radiation strikes and charge sharing effect, then they will be recovered. However, nodes "B" and "C" are insensitive to the radiation effect. This case looks like SEU on nodes "B," and "C" are recovered, as explained in subsection II-B (case -2, 4). Case 4 (SEDNU at node pair "B-D"): If the node pair "BD" is upset due to radiation strikes and charge sharing effect, they will be recovered. However, node "B" is insensitive to the radiation effect. This case looks like SEU on node "D" is recovered as explained in subsection II-B (case -3). Case 5 (SEDNU at node pair "C-D"): If the node pair "CD" is upset due to radiation strikes and charge sharing effect, they will be recovered. However, node "C" is insensitive to the radiation effect. This case looks like SEU on node "D" is recovered as explained in subsection II-B (case -3). Case 6 (SEDNU at node pair "A-D"): If more charge is placed at node pair "A-D," the cell's stored value may vary. The charge sharing among MOSs is minimal if their separation is greater than the effective range of charge sharing [4]-[9]. The proposed cell's layout is designed with suitable separation to avoid charge sharing among nodes. Hence, the proposed cell is SEU immune and SEDNU tolerant. It may be SEDNU immune if its layout maintains a minimum distance between sensitive node pairs, as reported in [5].

The proposed cell has the following advantages:
1) The proposed cell can self-recover at all the sensitive nodes from all the possible SEUs of both polarities. Also, it can self-recover from SEDNUs at its storage node. The more number of PMOSs in the proposed cell is responsible for better critical charge (Q_c) compared to other cells.
2) The proposed cell dissipates the lowest hold and total power due to the stacked structure. Also, in the proposed cell, the source of P5 and P6 transistors are connected to the gate of P3 and P4 (instead of supply voltage) to minimize power consumption, mainly in standby mode.
3) The proposed cell has better stability compared to most of the cells due to the lower body effect, better feedback path, high threshold MOSs (N1-N4), and better size of transistors.
4) The usage of PMOSs as pull-down transistors (P7-P10) and as access transistors (P1, P2) reduces the sensitive nodes and, therefore, the sensitive area of the proposed cell.
5) The writability and write access time are also improved compared to other SRAMs due to the better pull-up ratio and poor driving ability of their internal nodes. The use of low threshold (V_{th}) MOSs (P7-P10) in the proposed cell is also responsible for better writability and write access time.

4.3 Proposed Work Chapter 4:
MNU Resilience RHBD SRAMs

4.3.1 Soft-Error-Aware SRAM for Terrestrial Applications

In this work, we have proposed a low-cost, write enhancement soft-error-aware-14T (LWS14T) cell. The main benefit of the LWS14T is that it can solve the issue of single-node upset (SNU), as well as multiple-node upset (MNU) at the internal node. Soft errors such as SNU and MNU have become a

significant problem for SRAMs in aircraft and terrestrial applications. In this work, a novel low-cost and write enhancement soft-error-aware-14T (LWS14T) SRAM cell is proposed to provide sufficient protection against soft errors. The obtained observations demonstrate that the LWS14T can recover not only from SNUs but also from MNUs irrespective of the upset polarity. Furthermore, compared to considered RHBD cells, the LWS14T has reduced the cost in terms of power and delay. Also, the LWS14T gives a better critical charge, better stability, and better writability.

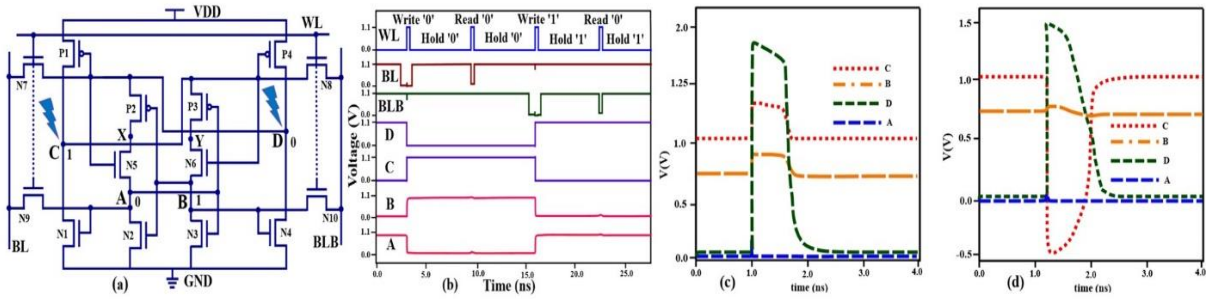

Fig. 6. (a) Circuit diagram, (b) Complete operational waveforms, (c) Simulated response for SNU recovery, and (d) DNU recovery of the proposed SRAM cell.

The schematic and transient responses of the LWS14T cell are depicted in Fig. 6(a) and (b), respectively. Assume '0' hold state for the LWS14T (i.e., "A" = "D" = '0', "B" = "C" = '1'). 1) Write Operation: To write '1' in the LWS14T, set the BL (BLB) to '1' ('0') and WL to '1'. BL (BLB) pulls nodes "A" and "D" ("B" and "C") up to VDD (down to GND). Also, as the value at "B" ("D") falls (rises), the intensity of the pull-down route, which corresponds to "A", diminishes, allowing "A" to charge fast. Once the voltage at node "A" goes just above the threshold voltage, N3 is switched ON. It facilitates quickly discharging "B". Similarly, the related access transistors alter the inner nodes to the required values. 2) Hold Operation: The WL is fixed to '0'. Thus, P1, P3, N2, N4, and N6 are turned ON, while the others are turned OFF. As a result, the cell remains constant in its initial condition. 3) Read Operation: The BL/BLB are pre-charged to '1', while WL is fixed to '1'. As a result, BL discharges via N9 and N2, whereas BLB stays at VDD since N3 is turned OFF. A sense amplifier completes the reading process.

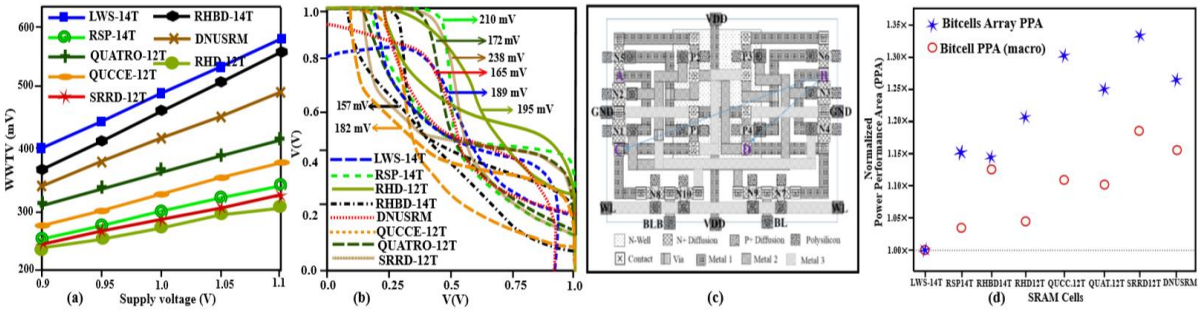

Fig. 7. (a) WWTV comparison at various VDD, (b) Butterfly curve in read mode, (c) Layout of the proposed cell, and (d) PPA comparison of SRAMs.

SNU at "D": If an SNU impacts "D", it changes from '0' to '1.' This switches OFF (ON) P1 (N5). Node "A," on the other hand, will maintain at '0' since unharmed node "B" keeps the P2 turned OFF. As a result of P1 and N1 being turned OFF, node "C" enters a high impedance condition and holds its value. As nodes "A," "B," and "C" retain their initial value, the cell is biased to return "D" to a logic '0' (Fig. 6(c)). MNU at "C-D": In this case, node "C" ("D") changes from '1' to '0' ('0' to '1'). This switches ON (OFF) N5, P4 (P1, N6). As "A" and "B" are cross-coupled inverted outputs, their levels cannot be altered without additional intervention. Hence, "A" and "B" preserve respective values. The node "B" ("A") maintains the N4 (N1) turned ON (OFF). As a result, "D" pulls down its value to '0'. This turned ON the P1. Therefore, "C" also pulled up its value to '1' (Fig. 6(d)). The primary factor of total power cost is leakage current [5]. In the LWS14T, the source of PMOSs P2 and P3 are connected to the gate of PMOSs P1 and P4 respectively instead of direct VDD. It gives less comparable current, which is

responsible for achieving less total power cost [8]. The proper selection of the size of transistors, an excessive amount of transistor stacking, and less wiring complexity are responsible for attaining less static power. The potential at the source of P2 and P3 are '0' and weak '1' rather than the VDD, respectively, during hold mode. Thus, it makes the NMOSs N5/N6 drain to collect charge hardly and gives less leakage current. The stability comparison of SRAMs for write mode and read mode is shown in Fig. 7(a) and (b), respectively. The layout of the LWS14T is shown in Fig. 7(c). The normalized PPA comparison for 8×8 bit cells array and macro operation (width of WL 0.4 ns) is shown in Fig. 7(d).

The following are essential characteristics of the proposed design:

1) The LWS-14T cell demonstrates better tolerance towards SNUs at all the sensitive nodes.
2) The MNUs generated at the internal node pair can also be healed using the LWS-14T cell.
3) The LWS-14T shows low static, total power cost, and better writability than other compared cells.
4) The write stability and write access time of the LWS-14T are also improved than other cells.
5) The read stability and access time of the LWS-14T is better than other cells.

4.3.2 Double-Node-Upset Aware SRAM Bit-cell for Aerospace Applications

In this work, an RHBD-13T SRAM cell has been proposed. This cell has been designed and verified using 5000 Monte Carlo (MC) simulations. It has been designed using thirteen transistors (five NMOS and eight PMOS transistors). The primary advantage of the proposed cell is that, due to its structural design, it is capable of self-recovery from DNUs. The proposed cell uses separate read and writes circuits to improve the speed of operation. In aerospace applications, the continuous scaling of CMOS technology makes SRAM cells more and more susceptible to soft errors. To overcome this issue, a radiation-hardened-based (RHBD) 13T SRAM cell has been proposed. The proposed cell has several benefits over other standard RHBD cells. The proposed cell can not only recover from SNUs induced at any of its sensitive nodes but also from DNUs induced at any of its sensitive node pairs. It has the lowest hold, total power cost, the highest critical charge, moderate area overhead, and better stability. To improve speed, the proposed cell uses a unique feedback path among its internal nodes. Finally, the figure of merit (FOM), and SNU probability of failure (POF) comparison of cells validate that the proposed cell is a better choice for sub-nanometer aerospace applications.

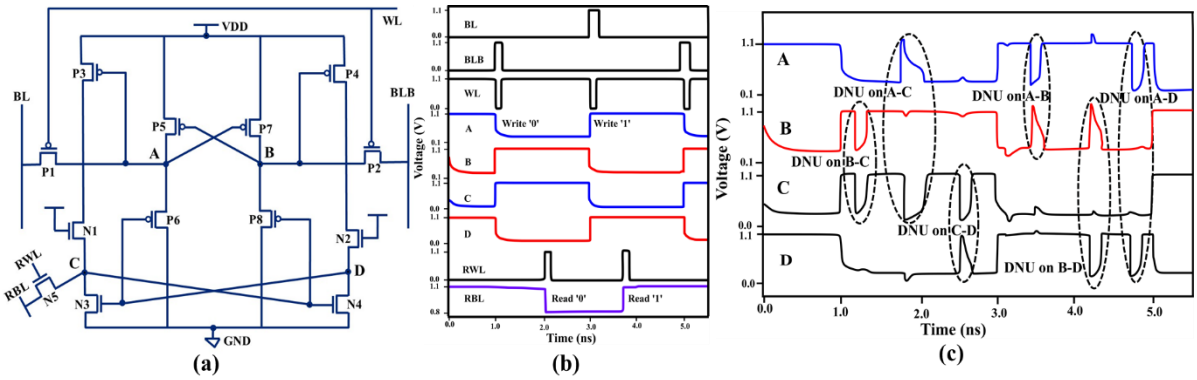

Fig. 8. (a) Circuit diagram, (b) Complete operational waveforms, and (c) Simulated responses for DNU recovery of the proposed RHBD-13T SRAM cell.

The circuit diagram of the proposed RHBD-13T bit-cell is presented in Fig. 8(a). The proposed 13T cell consists of eight PMOSs and five NMOSs. The access transistor P1 placed between the bit line (BL) and node "A" is driven by a word line (WL). Similarly, P2 placed between BLB and node "B" is driven by WL. The PMOS access transistors (P1, P2) are used to improve reliability, but they can reduce the read access time. Hence, in the proposed cell, the separate read access transistor N5 is used between the read bit line (RBL) and node "C" operated by the read word line (RWL). The complete transient responses and DNU recovery of the proposed cell are shown in Fig. 8(b) and (c), respectively. The proposed cell uses a low threshold voltage (V_{th}) operated by an NMOS transistor N1 between P3 and N3. Similarly, the low threshold NMOS transistor N2 is used between P4 and N4. The transistors P6, P8, N1, and N2 (N3, N4) in the proposed cell are taken as high (low) V_{th} MOSs. The use of low V_{th}

transistors (N1, N2) in the proposed cell increases the voltage swing of the output. Simultaneously, the high V_{th} NMOSs (N3, N4, P6, and P8) reduce the leakage current, minimize power loss, and improve stability. The junctions between PMOSs P5, P6, and P1 (P7, P8, P2) in the proposed cell are denoted as node "A" ("B"). Similarly, the junctions between NMOSs N1, N3, and N5 (N2, N4) in the proposed cell are marked as node "C" ("D"). The nodes "A" and "B" are '1' to '0' flip immune as nodes are surrounded by PMOSs. Similarly, nodes "C" and "D" are '0' to '1' flip immune as NMOSs are surrounded them [12]-[15]. The overhead comparison of SRAMs is reported in Table III.

Table III: Overhead comparison of SRAMs

SRAM Cells	SNUR	DNUR	Static Power (nW)	Total Power (μW)	Area (μm^2)	RAT (ps)	WAT (ps)	Percentage Reduced Cost of Proposed Cell (%)				
								ΔSP	ΔTP	ΔA	ΔR	ΔW
Proposed-13T	√	√	**26.83**	**2.12**	**1.596**	**78.11**	**11.93**	**-**	**-**	**-**	**-**	**-**
RSP-14T [9]	√	√	33.02	2.71	1.778	88.78	13.36	18.75	21.77	10.24	12.02	10.70
RHBD-14T	√	√	34.21	2.64	1.701	93.51	11.89	21.57	19.69	6.17	16.47	-0.33
RHBD-13T [8]	√	√	45.32	2.98	1.672	85.01	21.02	40.79	28.86	4.54	8.12	43.24
QUC.-12T [5]	×	×	41.02	4.51	1.478	81.52	19.23	34.59	52.99	-7.39	4.18	37.96
RHBD-12T [6]	√	×	32.82	2.56	1.432	91.32	10.23	18.25	17.18	-10.3	14.46	-14.2
QUAT.-12T [3]	×	×	38.23	3.73	1.492	76.13	16.81	29.82	43.16	-6.52	-2.53	29.03
DICE-12T [1]	√	×	36.52	2.93	1.581	83.30	14.21	26.53	27.64	-0.94	6.23	16.04

SNUR: Single node upset resilience, DNUR: Double node upset resilience

Overall, the proposed cell offers the following benefits:
1) The proposed cell can self-recover at all the sensitive nodes from all the possible SNUs of both polarities. It has the highest SNU critical charge among all considered cells.
2) The proposed cell can self-recover at all the sensitive node pairs from all the possible DNUs of both polarities.
3) The proposed cell has better stability due to the better feedback path and transistors size.
4) The proposed cell dissipates the lowest hold and total power cost due to stacked structure and weak PMOS transistors in the pull-down path.
5) The write and read speeds are also improved compared to other cells due to lower body effect, feedback path, and extra access transistors (N5).

4.4 Proposed Work Chapter 5:
Soft Error Resilience MRAM Memory

4.4.1 Memory Cell Design using Hybrid CMOS and MTJ

This work presents optimal 1T-2MTJ STT-MRAM cell architecture with a low threshold voltage NMOS transistor as an access device. Memory is an essential component of any VLSI data storage system. Because of the shrinking of CMOS processing nodes, power consumption in conventional memory (SRAM, DRAM) increases. Traditional memory technologies also suffer several additional difficulties, such as limited scalability, low reliability, short data retention time, low durability, increased space, and latency, among others. As a result, new device technologies are critical for developing low-power, high-performance memory devices. Among the numerous developing Non-volatile (NV) memory technologies available today, STT-MRAM is regarded as one of the most appealing and promising non-volatile memory technologies for overcoming the limitations of traditional memories. STT-MRAM is more efficient, quicker, non-volatile, highly scalable, and readily integrated with CMOS technology. Due to the scalability of technology nodes below 45nm, traditional STT-MRAM cells have several difficulties, including high write power consumption, destructive read and write operation and prolonged write time. To address the issues associated with the writing operation of STT-MRAM cells, this work presented an optimum STT-MRAM cell design based on PMA-MTJ. The write failure mitigation strategies are utilized to increase the proposed cell's write stability. A comparative analysis between the conventional STT-MRAM cell and the proposed cell is

performed. As from analysis, the write power dissipation in conventional STT-MRAM cells is increased as the size and the threshold voltage of an access transistor increase. In this regard, a low threshold voltage NMOS transistor is employed for lowering the power consumption and delay during the write operation of the STT-MRAM cell. Due to the low write current, the presented cell has less write stability. To reinforce the write stability of the proposed STT-MRAM cell architecture, the failure mitigation techniques proposed in [17]-[22] are considered.

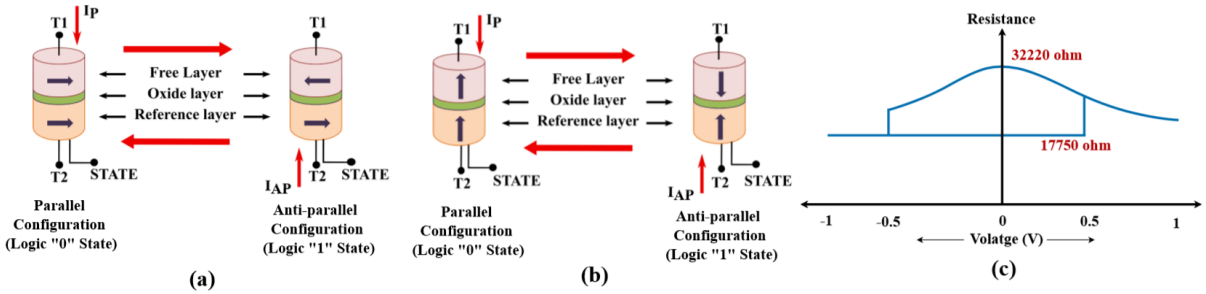

Fig. 9. Structure of MTJ, its configuration, and STT switching mechanism; a) IP-MTJ, b) PMA-MTJ; a positive current (IP) flowing from terminal T1 to terminal T2 changes MTJ state from parallel to the antiparallel and current flowing from T2 to T1 make change the state of MTJ from antiparallel to parallel state, and (c) R-V hysteresis loop of PMA-MTJ; for VDD = 1V, the PMA-MTJ offers the resistance in antiparallel state RAP = 32220 ohm and in parallel state RP = 17750 ohm.

STT-MRAM uses the principle of spintronics to write the data in MTJ. The STT is the most widely used switching approach. In this approach, a spin-polarized current is utilized for flipping the spin of electrons which successively alters the magnetic direction of magnetic layer (FL). This technique offers high power efficiency and fast writing speed [16]. An electric current that is generally unpolarised produces a spin-polarized current. Firstly, this current passes across a thick magnetic layer which is RL. When this spin-polarized current is more than the switching threshold current of MTJ, it penetrates the oxide layer and enters into a thinner magnetic layer (FL). Then the angular momentum is transferred to FL due to the magnetic direction of FL changing either parallel or antiparallel concerning RL. When this current passes from the FL to the RL, the antiparallel-to-parallel switching happens while in the case of parallel-to-antiparallel switching, this current passes from the RL to the FL. The switching mechanism of IP-MTJ and PMA-MTJ is illustrated simply in Fig. 9(a) and (b). Fig. 9(c) depicts the resistance-voltage (R-V) hysteresis loop of PMA MTJ using the STT switching mechanism. The R-V curve can be obtained by sweeping the MTJ voltage from 0 to VDD for parallel (P) to antiparallel (AP) switching and - VDD to 0 for antiparallel (AP) to parallel (P) switching. It is the DC characteristic curve of the device which gives comprehensive information on the MTJ characteristics, such as the RP, RAP, and TMR values. Also, the switching operation can be clearly understood with the R-V curve of the device as shown in Fig. 9(c).

The proposed STT-MRAM cell incorporates two MTJs to store the one-bit information, as shown in Fig. 10(a). An NMOS transistor is connected in series with parallel-connected MTJs to give enough current to flip the states of both MTJs. As mentioned within the preceding Section, the conventional STT-MRAM cell faces high power consumption and delay for a write operation. Thus, to reduce that, a low threshold NMOS transistor is employed. The current required to write the data bit decreases because of the low threshold voltage of NMOS. Due to this, the power consumption during writing operations reduces considerably. Also, the delay incurred by the presented STT-MRAM cell is decreased due to the low threshold voltage of NMOS.

From Fig. 10(a), the MTJ consists of three terminals. The two terminals are T1, T2, and the real terminals of MTJ, where the bidirectional signal is applied for switching the magnetic state of MTJ. These two terminals aren't bilaterally symmetrical, a positive current coming into T1 will create the state change from the antiparallel state ("1") to the parallel state ("0"), and a positive current coming into terminal T2 will create the state change from a parallel state ("1") to antiparallel state ("0"). T1 is connected to the bit-line (BL) from where the data bit that has to be written in MTJ is applied. T2 of both MTJs are connected to the drain terminal of the NMOS. The third terminal STATE is the virtual

terminal that is utilized for determining the state of MTJ and is associated with the source line (SL) of the NMOS transistor through a resistor. The Word line (WL) is connected to the gate terminal of the NMOS transistor that controls the operation performed by the STT-MRAM cell. The transient responses of the write operation of the proposed STT-MRAM cell are shown in Fig. 10(b). For write margin calculation, the R-V hysteresis curve is shown in Fig 10(c).

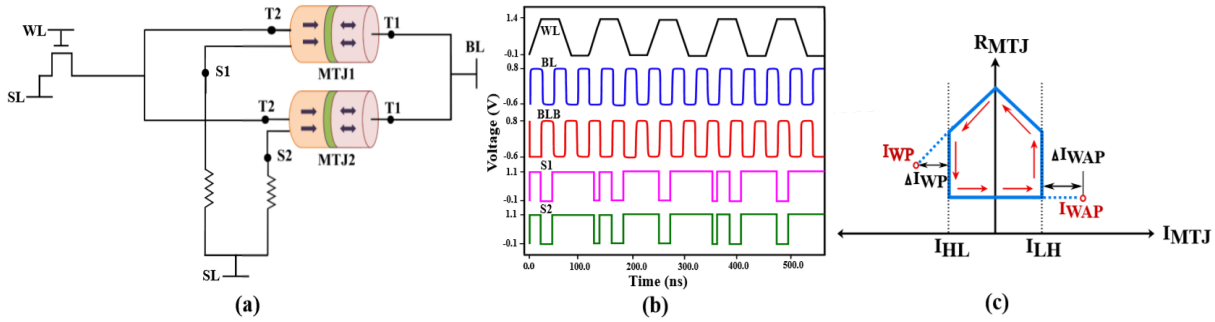

Fig. 10. Schematic of the proposed STT-MRAM cell, (b) Transient response of write operation of the proposed STT-MRAM cell, and (c) Write Margin for write "0" (ΔIWP) and write "1" (ΔIWAP).

The highlights of our contributions can be summarized as follows:
1. A 1T-2MTJ cell architecture with a low threshold voltage NMOS transistor is introduced to address the issues such as high power consumption and low speed during the write operation of the conventional STT-MRAM cell architectures.
2. To improve the write stability, the two techniques, transistor body biasing and word line voltage boosting, are adopted in this proposed cell.
3. Circuit simulations of conventional and proposed STT-MRAM cells are performed in the Cadence Virtuoso Tool. The simulated results validated the efficiency of the presented STT-MRAM cell.
4. A comparative analysis between conventional and proposed STT-MRAM cells has been performed concerning delay, power, and stability during the write operation.

4.4.2 Soft-Error-Tolerant Non-volatile MRAM Memory

Field-programmable gate arrays based on static random access memory are more prevalent than other varieties, including flash and anti-fuse, due to their limitless configurability and excellent performance. It becomes more critical for CMOS circuits to have a low standby power consumption. Magnetic RAM (MRAM) logic circuits can be an excellent alternative to SRAM-based logic because they have no leakage and can work with CMOS. Furthermore, MRAM logic in FPGA designs rather than SRAM logic provides several additional benefits, including non-volatility and high radiation dependability.

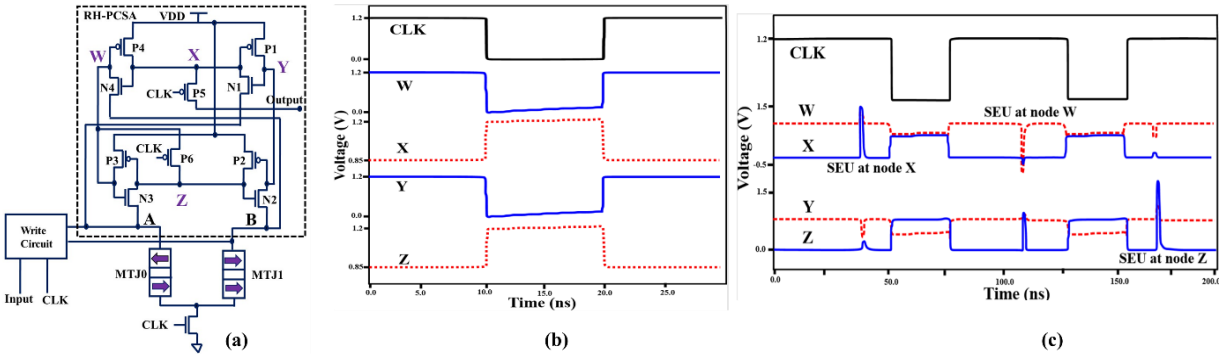

Fig. 11. (a) Proposed rad-hard M-RAM, (b) Normal operation of the proposed rad-hard M-RAM, Nodes X1–X4 versus clock signal. (c) SEU recovery of the proposed RH-PCSA circuit.

In this work, the effects of radiation-induced soft errors on MRAM are taken into account. The soft error tolerance of the previous MRAMs is discussed, and a new MRAM structure is proposed. Non-volatile, low-power, high-speed MRAM is resilient to soft errors. The proposed MRAM with high

radiation resilience has a low design overhead compared to existing comparable MRAMs is reported in Table IV. The proposed MRAM shows the single node upset tolerance.

Table IV: Comparison of the Proposed M-RAM (TSMC 65 nm CMOS Model and the Spice-MTJ Model of [20])

M-RAM Circuit	MTJ Count	CMOS Count	SEU Tolerant	Recovery Time (20 fc) (nS)	Total Power (μW)	Static Power (nW)	Read Latency (nS)	Read Energy (pJ)
Proposed 11T	**2**	**11**	**Yes**	**0.64**	**8.6**	**19.5**	**0.25**	**2.6**
27T M-RAM	8	27	Yes	1.11	46.8	35.7	0.20	5.62
26T M-RAM	4	26	Yes	1.23	28.9	36.2	0.21	5.23
21T M-RAM	2	21	Yes	0.72	9.3	31.7	0.26	3.25
13T M-RAM	2	13	Yes	0.61	9.8	28.5	0.25	2.89
13T M-RAM	2	13	Yes	0.83	10.5	26.9	0.26	3.77
7T M-RAM	2	7	No	-	6.5	17.2	0.20	1.81
17T M-RAM	4	17	No	-	24.5	32.2	0.24	2.36

The RAMs are an integral part of the FPGA logic block. In half of the clock cycles, this circuit is transparent (read). So its radiation resistance is required [18]. Fig. 11(a) shows a radiation-tolerant M-RAM circuit. This circuit uses two MTJs and one 11-transistor PCSA (the so-called RH-PCSA circuit). Nodes W and Y (and X and Z) always have the same logic state. Figure 11(b) shows that when the clock signal is strong, nodes X and Z go high while nodes W and Y go to zero. Due to MTJ1 being in parallel mode and having a lower resistance than MTJ0, a pull-down channel from this MTJ (N5 to ground) is formed, causing nodes W and Y to zero. Fig. 11(b) shows the circuit in normal operation. In Fig. 11(b), nodes W–Z are depicted in both clock signal modes. Fig. 11(c) shows SEU injection and tolerance in nodes W-Z of the proposed rad-hard PSCA circuit.

As seen in Figure 11(a), nodes W and X of the proposed rad-hard PCSA circuit contain a dual node consisting of Y and Z, respectively. If an energetic particle damages one of these nodes, the PCSA circuit can return to its original state since the dual node is not damaged. As a result, SEU will not occur because the PCSA circuit can recover its original state. Once the clock signal is high in the configuration shown in Fig. 11(a), transistors N2, N4, P4, and P3 are turned ON, causing W and Y to remain at zero. Since P1 and P3 are in the OFF state and their drain terminals are linked to N2 and N4, respectively, an energetic particle impacting N1 or N3 might affect the area that was struck. If a particle strikes P3 and causes a momentary change at the logic level of W (from 0 to 1), no change will occur at N4 and P3 since X will stay securely at 1. As a result, the principal logic value of W will remain unchanged. If an energetic particle has an effect on N1 and changes the value of X to zero, the ON-state P1 will restore it to its original condition.

5. Major Contributions of the Work:

Some of the significant contributions of the work are:

I. The prevalent radiation-hardened-based SRAMs suffer from a large number of write failures under temperature and process variations of sub-nanometer CMOS technology. Therefore, both boosted word-line and bit-line have been proposed to improve the writability of SRAMs.
II. An RHBD SARM cell has been proposed to overcome the soft errors (single event upset) and writability failure issue at a higher frequency under process variations.
III. A single event double node upset tolerant SRAM has been proposed to overcome the single event double node upset. The SEDNUT SRAM can self-recover at all the sensitive nodes from all the possible SEUs of both polarities. Also, it can self-recover from SEDNUs at its storage node. The layout optimization technique has been used in the proposed SEDNUT SRAM to minimize the charge-sharing effect and improve the voltage swing.
IV. A low-cost and write enhancement soft-error-aware-14T (LWS14T) SRAM is proposed to provide sufficient protection against single node upset and multi-node upset (MNU)

irrespective of the upset polarity. Also, the LWS14T gives a better critical charge, better stability, and better writability.

V. Double-Node-Upset Aware SRAM Bit-cell has been proposed to recover from all the possible single and double node upsets with a better balance of all other parameters. The proposed cell uses separate read and write circuits to improve the speed of operation and read stability.

VI. An optimum STT-MRAM has been designed To address the difficulties such as limited scalability, lower liability, short data retention time, low durability, increased space, and latency by traditional memory. The proposed radiation-hardened MRAM showed that it can tolerate soft errors. The proposed soft error-tolerant, low-power, non-volatile, and high-performance MRAMs incur a little overhead while offering complete robustness against SEUs.

6. Conclusion and Future Scope:

The complete work demonstrates the soft error-aware RAMs to address the challenges associated with RAMs at advanced technology nodes. The proposed SNU, SEDNU, and MNU tolerant SRAMs provide a better balance among all the parameters at a low voltage region, making them a better choice for low voltage terrestrial and aerospace applications. Also, the proposed SRAMs have been verified using Monte–Carlo simulation in CMOS technology. The Magnetic-based circuits offer some attractive features such as low standby power and non-volatility. As SRAM-based memories suffer from high standby power consumption as well as volatility, magnetic-based memories are suggested as their alternative replacement in the literature. STT-MRAM can offer some advantages of non-volatility, almost zero leakage power, and high-performance computing. However, they are still vulnerable to radiation-induced soft errors. In this work, a radiation-hardened MRAM has also been proposed. The proposed soft error-tolerant, low-power, non-volatile, and high-performance MRAM incurs a slight overhead in design while offering complete robustness against SEUs.

The future work objectives are to discover the compact random access memory design concerning the state-of-the-art design possibilities. Some of the future scopes are listed below:

1. The work can be extended to fabricating and testing soft-error-aware RHBD SRAM and MRAM-based memory.
2. There are still several challenges like write failure and process variation associated with the RHBD RAMs for very low voltage and high-frequency applications.
3. This work can be extended to overcome the challenges related to the single event double node upsets and multi-node upsets in MRAMs.
4. Further, the work can provide the future direction to understand the reduction of write energy in MRAM-based memory.
5. The MNU tolerance SRAM are SNU and SEDNU tolerance irrespective of upset polarity at all the nodes. However, it is MNU tolerance only for storage nodes. Hence the multi-node upset aware SRAM at all the nodes can be further re-investigated with optimized parameters.
6. The soft error resilience MRAM-based work gives only SNU tolerance. This work can be extended to overcome the challenges related to the single event double node upsets and multi-node upsets in MRAMs.

7. Organization of the Thesis:

A brief outline of each chapter is given below:

I. **Chapter-1**: This chapter discusses the basic introduction and state-of-the-art RHBD random access memories. Apart from that, it consists of different types of soft errors. The chapter covers the effect of radiation particles on circuits, types of radiation hardening, comparison of different RHBD RAMs, challenges in soft error tolerant RAMs, motivation, and objectives. Additionally, the Thesis organization and major contributions have also been detailed.

II. **Chapter-2:** This chapter describes soft errors like single-node upset resilience SRAM for low voltage applications and boosted word line and bit line on SRAM to improve the writability of the SRAM for higher frequency and lower node applications. Further, the single node upset resilience SRAM bit-cell has been proposed and compared with other SRAMs in terms of power, stability, area, and soft error resilience for higher frequency. **Publications: [5] & [7]**.

III. **Chapter-3:** This chapter proposes soft errors like single event double node upset resilience SRAM bit-cell for low voltage space applications. The charge sharing effect among MOSs leads to a single event double node upset in SRAMs, especially for lower node technology. Hence, further in this work, the charge sharing effect has been analyzed for SRAMs. Finally, the statistical analysis of the SRAMs validated the proposed work. **Publications: [2] & [6]**.

IV. **Chapter-4:** This chapter deals with soft errors like multi-node upset tolerant SRAM-based memory. In this Chapter, double-node-upset aware SRAM bit-cell for aerospace applications has been proposed. This cell has been designed and verified using 5000 Monte Carlo simulations. Further, a low-cost, write enhancement multi-node-soft-error-aware-14T-based memory has been proposed. The multi-node upsets recoverability of the proposed SRAM irrespective of the upset polarity has been discussed in this Chapter. **Publications: [1] & [3]**.

V. **Chapter-5:** This chapter introduces the significance of emerging devices like STT-MRAM-based memory. In this chapter, the one-transistor, two MTJ-based STT-MRAM has been proposed and compared with many other conventional STT-MRAMs. Further, in this Chapter, the effects of radiation-induced soft errors on MRAM are taken into account. The soft error tolerance of the previous MRAMs is discussed, and a new MRAM structure is proposed. **Publications: [4] & [10]**.

VI. **Chapter-6:** This chapter highlights the conclusion and future work. General summary, limitations, and related future work are incorporated in this section.

8. Publications from the Work

Patent Submitted:

[1] Govind Prasad, Bipin Chandra Mandi, and Maifuz Ali, "Computing Device having 14T SRAM Cells for Aerospace and Terrestrial Applications," (Application no.-202221021159).

[2] **Govind Prasad**, Bipin Chandra Mandi, and Maifuz Ali, "sETNM: Soft-Error-Tolerant Non-volatile MRAM for Terrestrial Applications," (Communicated).

Published Journal(s):

[1] **Govind Prasad**, Bipin Chandra Mandi, and Maifuz Ali, "Highly Reliable Low Cost, Double-Node Upset Tolerant Radiation Hardened SRAM Bit-cell for Aerospace Applications," *Micro. Reliability Journal, Elsevier*, vol. 133, 114526, Jun. 2022. DOI: 10.1016/j.microrel.2022.114526

[2] **Govind Prasad**, Bipin Chandra Mandi, and Maifuz Ali, "Energy-Efficient Radiation Hardened SRAM Cell for Low Voltage Terrestrial Applications," *Microelectronics Journal, Elsevier*, vol. 120, 105340, Jan. 2022. DOI: 10.1016/j.mejo.2021.105340

[3] **Govind Parsad**, Bipin Chandra Mandi, and Maifuz Ali, "Soft-Error-Aware SRAM for Terrestrial Applications," ***IEEE Transactions on Device and Materials Reliability***, vol. 21, no. 4, pp. 658-660, Oct. 2021. DOI: 10.1109/TDMR.2021.3118715

[4] **Govind Prasad**, D. Sahu, Bipin Chandra Mandi, and Maifuz Ali, "Novel Low Power and Stable Memory Cell Design using Hybrid CMOS and MTJ" *Journal of Circ. Theory and Applications, Wiley*, vol. 49, no. 12, pp.1-12, Dec. 2021. DOI: 10.1002/cta.3204

[5] **Govind Prasad**, Bipin Chandra Mandi, and Maifuz Ali, "Low Power and Write-Enhancement RHBD 12T SRAM Cell for Aerospace Applications" *Intern. Journal of Analog Integrated Circuits and Signal Processing, Springer*, vol. 107, pp. 377-388, Jan. 2021. DOI: 10.1007/s10470-020-01786-8

[6] **Govind Prasad**, Bipin Chandra Mandi, and Maifuz Ali, "Power Optimized SRAM Cell with High Radiation Hardened for Aerospace Applications," *Microelectronics Journal, Elsevier*, vol. 103, 104843, Sep. 2020. DOI: 10.1016/j.mejo.2020.104843

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Under Review-Journal(s):

[8] Govind Prasad, Bipin Chandra Mandi, and Maifuz Ali, "Energy-Optimized and Soft-Error-Aware Read- Decoupled SRAM for Aerospace Applications," *IEEE Trans. Devi. Mat. Rel.*. (Under Review)

[9] Govind Prasad, Bipin Chandra Mandi, and Maifuz Ali, "SRAM Cell with Enhanced Self Recoverability from Soft Errors for Terrestrial Applications," *IEEE Trans. VLSI* (Under Review)

[10] Govind Parsad, Bipin Chandra Mandi, and Maifuz Ali, "Soft Error Aware Non-Volatile MRAM based FPGA," *IEEE Trans. on Magnetics*. (Ready to Send)

Published Conference(s):

[11] **Govind Prasad**, Prachi Humne, Bipin Chandra Mandi, and Maifuz Ali, "Design and Analysis of Optimal SRAM Cell using CMOS and Emerging Devices," *in Proc. IEEE Int. SPIN-2021*, Delhi, India.

[12] **Govind Prasad**, Dulari Tandon, Bipin Chandra Mandi, and Maifuz Ali, "Process Variation Analysis of 10T SRAM Cell for Low Power, High-Speed Cache Memory for IoT Applications", *in Proc. IEEE 7th Int. SPIN-2020*, Delhi, India.

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